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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,534	01/29/2001	John Appleby-Alis	EMB1P022	9218

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EXAMINER	
THOMSON, WILLIAM D	

ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/772,534	APPLEBY-ALIS ET AL.
	Examiner	Art Unit
	William D. Thomson	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2001 and 03 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented for examination.

2. Claims 1-21 have been examined and rejected.

Priority

3. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. The priority date of July 20th, 2000 has been used during the examination of the instant case.

CLAIMS

4. Claims 5, 12, and 19 are objected to as having minor informalities as follows:

The word "FPGA's" is cast as possessive, it appears to be a typographic error and should be amended to the plural usage, i.e. FPGAs.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. §102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-21 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Sugiyama (047).

Taking claim 1, for example, Sugiyama (047) teaches a method for network-based configuration of a programmable logic device (see figure 2, for example), comprising the steps of:

initiating a default application on a programmable logic device (FPGA or PLD)

sending a file request (connecting to host) for configuration data from the logic device to a server located remotely (Host computer 2 or distribution center 4) from the logic device utilizing a network (communications network or telephone line)

receiving the configuration data from the network server (Host computer 2 or distribution center 4 transmitted to the electronic apparatus 1)

utilizing the configuration data for configuring the logic device to run a second application (effects or FIR or IIR); and

running the second application on the logic device at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 2, the method of claims 1, wherein the configuration data is received in the form of a bit file (bit stream stored locally in memory 11) is taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 3, the method of claim 1, wherein the logic device includes at least one FPGA (FPGA 33 or 34 or alternately PLD 15 or 16) is taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 4, the method of claim 3, wherein a first FPGA receives the configuration data, wherein the first FPGA configures a second FPGA utilizing the configuration data is taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 5, the method of claim 3, wherein the logic device includes first and second FPGAs (FPGAs 33 and 34 or alternately PLDs 15 and 16) that are clocked at different speeds (clocking speed is inherently dependent on configuration of programmable logic, with two different devices implementing two different configurations they will clock differently) as taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 6, the method of claim 1, wherein the default application and the second application are both able to run simultaneously on the logic device (application on one FPGA 33 or PLD 15 and another application on FPGA 34 or PLD 16) is taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

As to claim 7, the method of claim 1, wherein the logic device further includes at least one of a display screen (20 or 41), touch screen (20 or 41), an audio chip (tone generator 32 – fig 3), an Ethernet device, a parallel port, a serial port (UART 12 in fig – 1, interface FPGA 39 connectivity with other peripherals 42, communications controller 37 – fig 3), a RAM bank (memory 11 –fig 1), and a non-volatile memory (31 or 40) is taught at Figures 1-5, Abstract, col. 2, lines 62 et seq.

6. Claims 8-21 are rejected based upon the same reasoning as claims 1-7, *supra*. Claims 8-21 are program product and system claims reciting the same invention as

claimed in method claims 1-14 as taught in Sugiyama at Figures 1-5, Abstract, col. 2, lines 62 et seq.

Conclusion

7. The prior art made of record, see accompanying P.T.O 892, and not relied upon is considered pertinent to applicant's disclosure.

CONTACT INFORMATION

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 703-305-0022. The examiner can normally be reached on 8:30-3:30 Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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